

FIG. 1

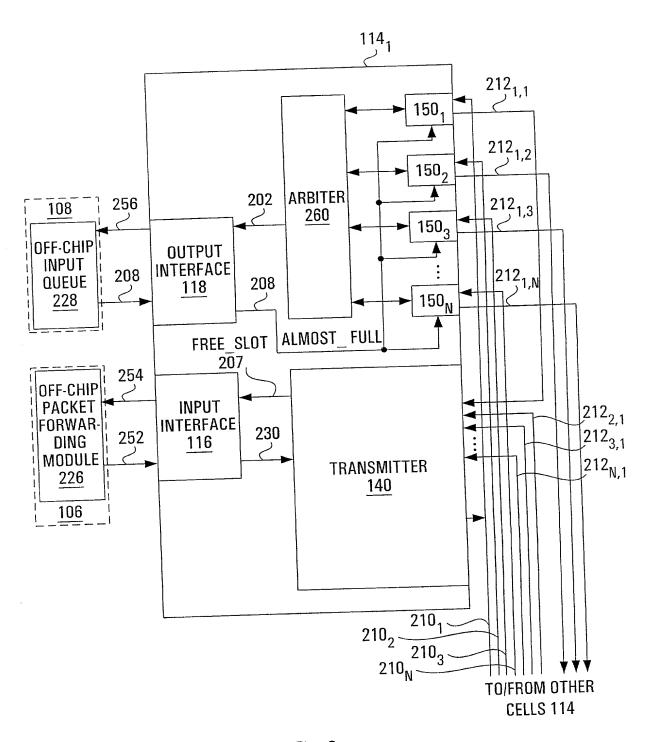


FIG. 2

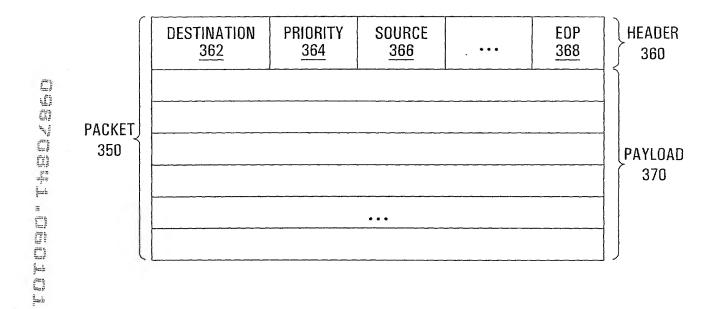


FIG. 3

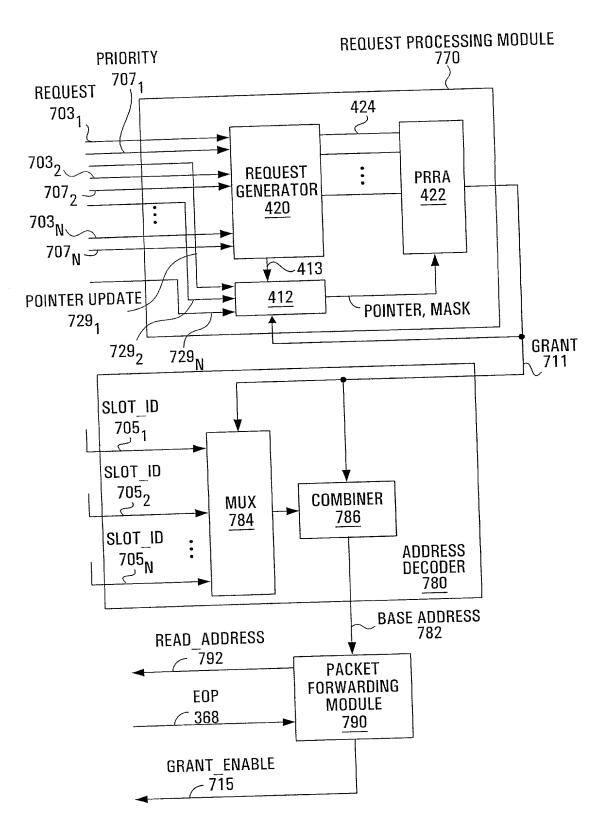
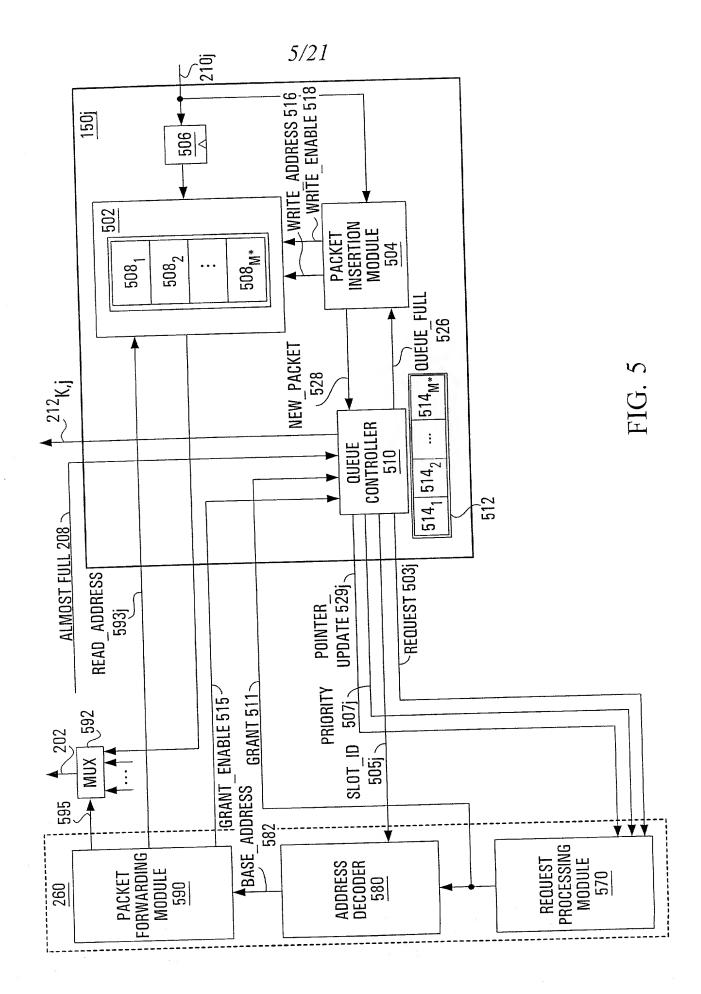


FIG. 4



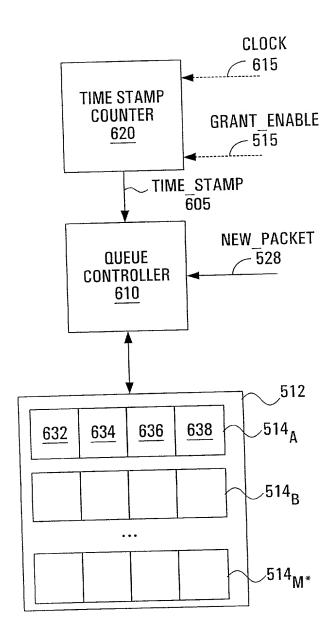
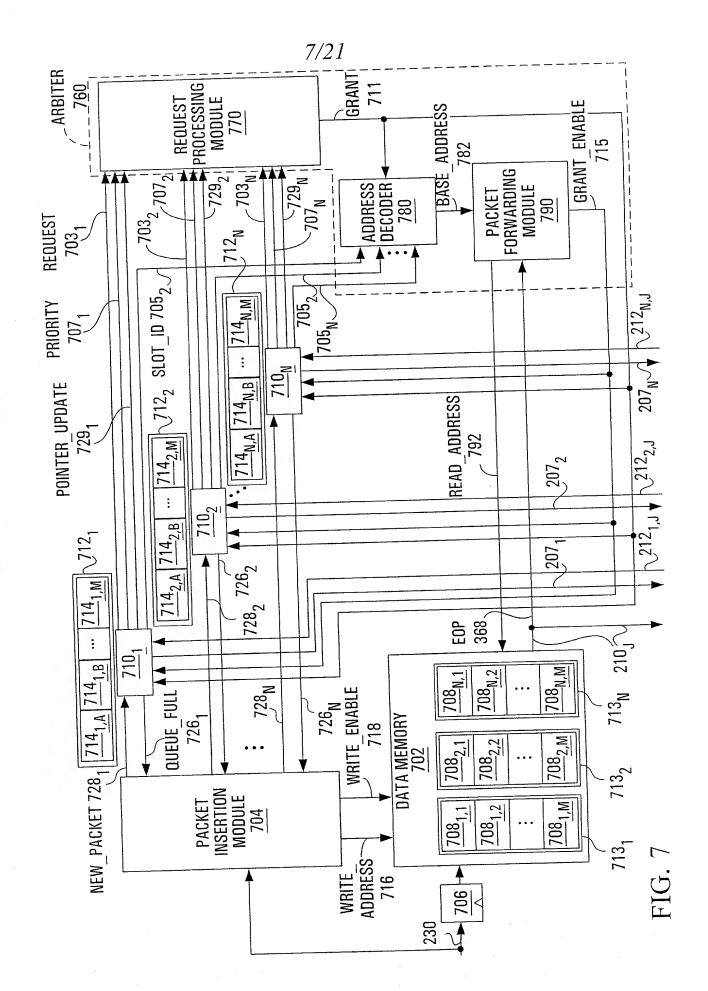
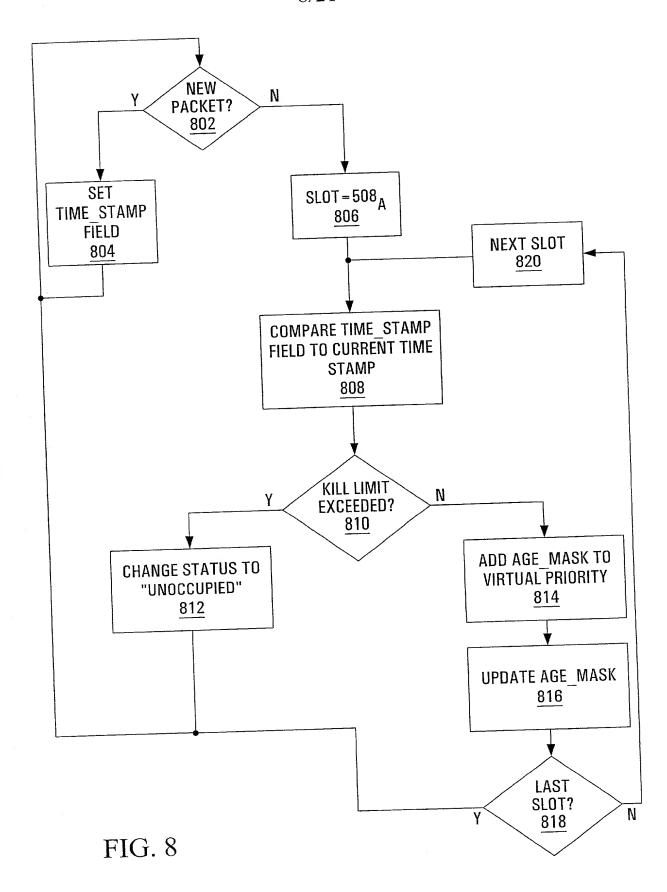


FIG. 6





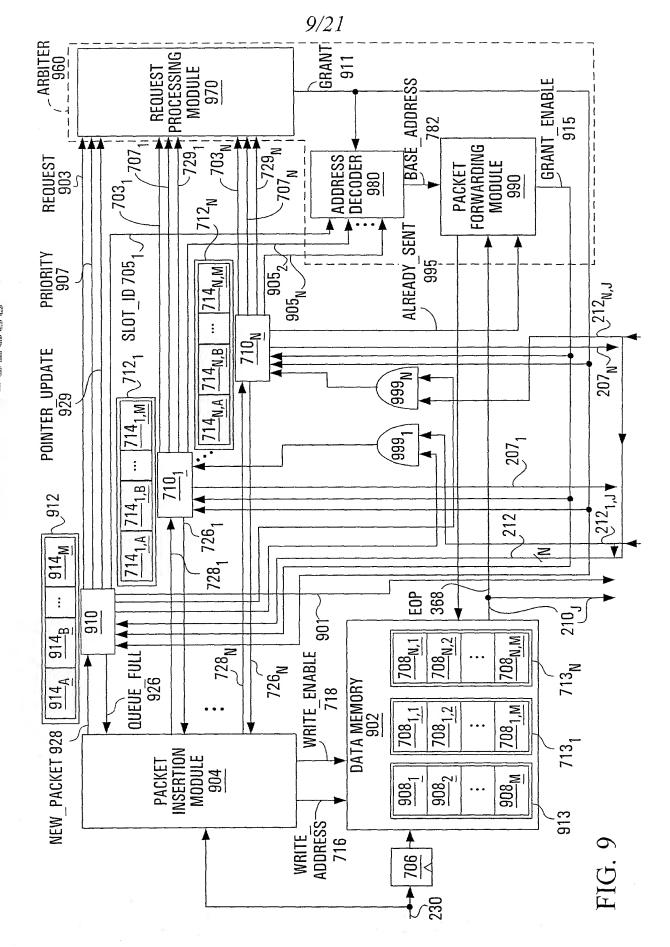


FIG. 10

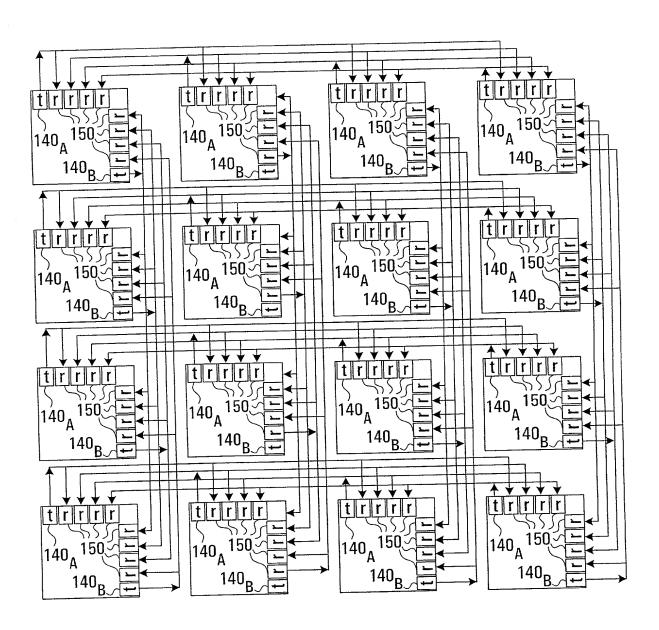


FIG. 11

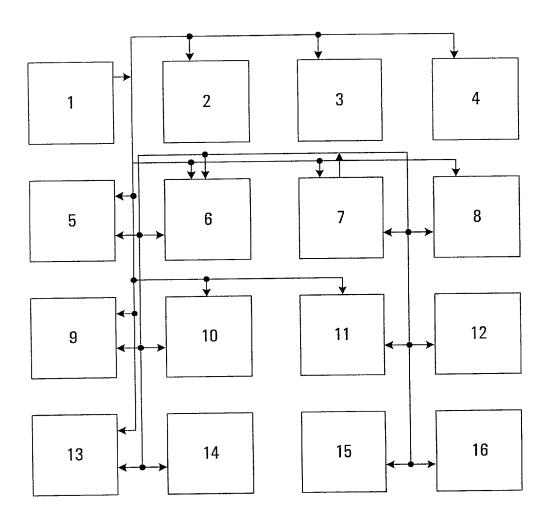
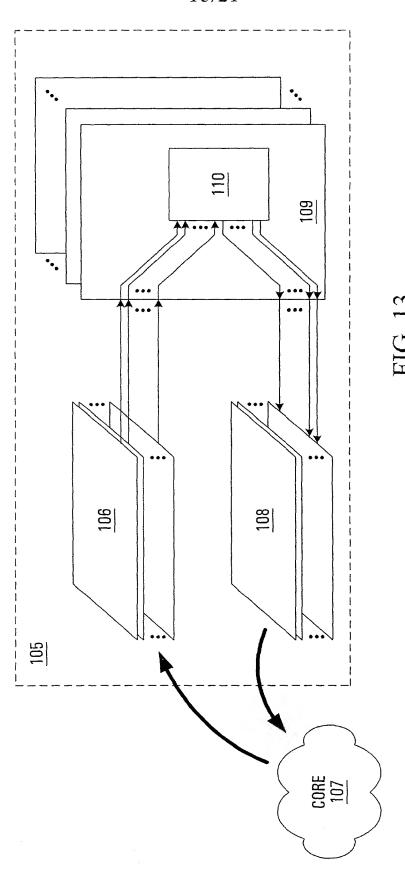
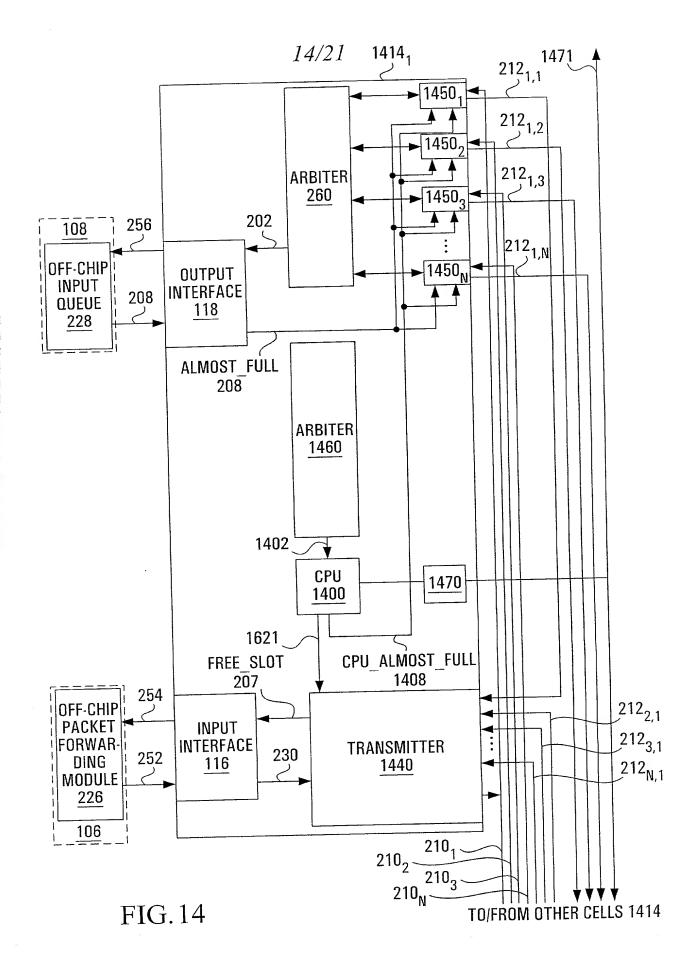


FIG. 12





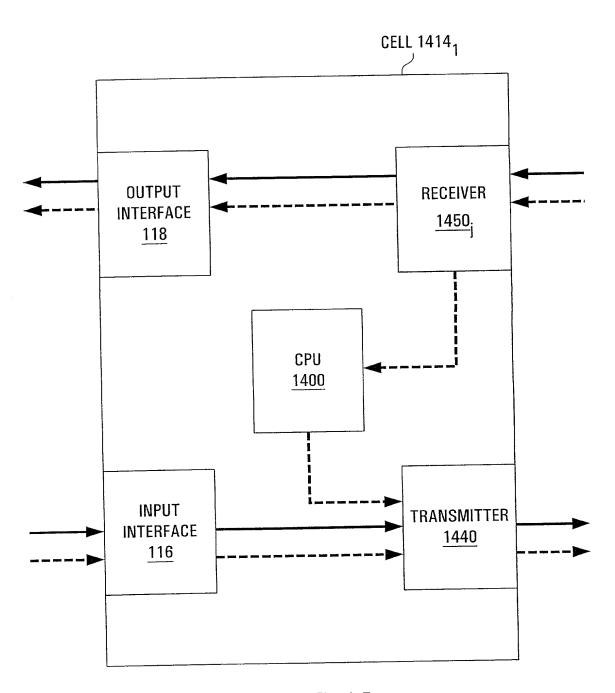
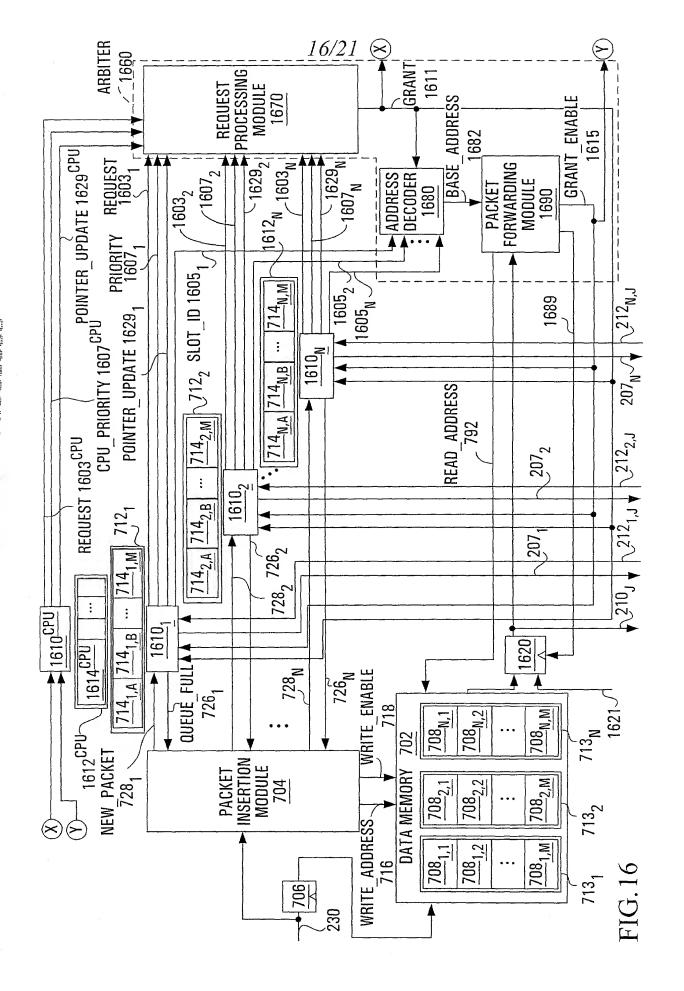


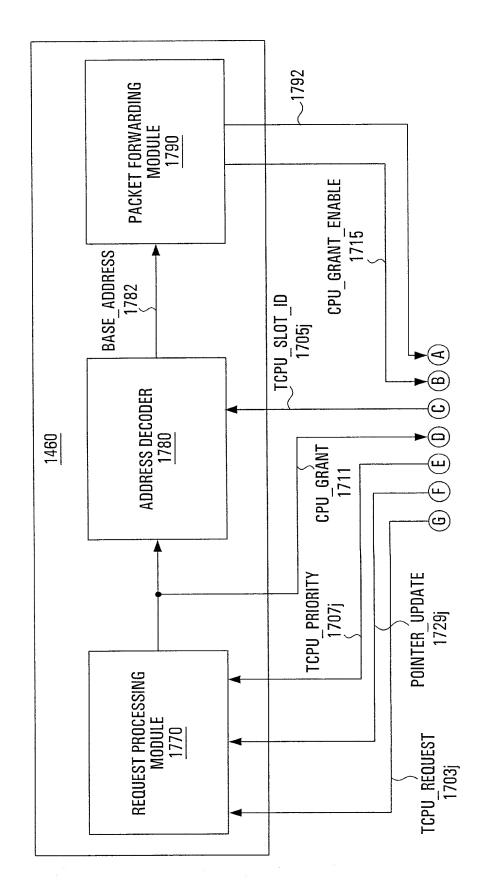
FIG. 15



17/21 21⁰j WRITE ADDRESS 516 1450 206 1450j 1702 PACKET INSERTION MODULE 1704 508_M* 1708 508_{2} 508, CPU_ALMOST_FULL NEW PACKET QUEUE_FULL 526 __ READ_ADDRESS 1793j 514_{M*} 1714 1408 QUEUE CONTROLLER 1710 ALMOST FULL 5142 208 514, 1795 $\overline{\mathbf{C}}$ (<u>a</u> UPDATE 529j~ 1712 -REQUEST 503j -GRANT 511 POINTER 1794 GRANT_ENABLE 515 (0) PRIORITY 507 202 1792 SLOT ID X∩W ▲ **→** $50\overline{5}$ -1791 592 ABASE ADDRESS 582 PROCESSING MODULE 570 PACKET FORWARDING DECODER 580 MODULE 590 ADDRESS REQUEST 260

FIG. 17A

FIG. 17B



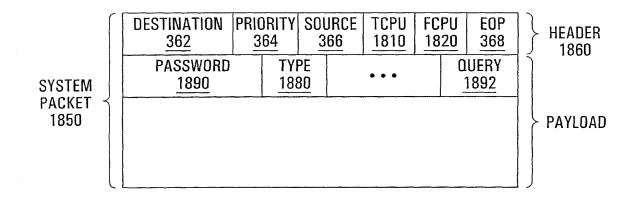


FIG. 18

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FIG. 19

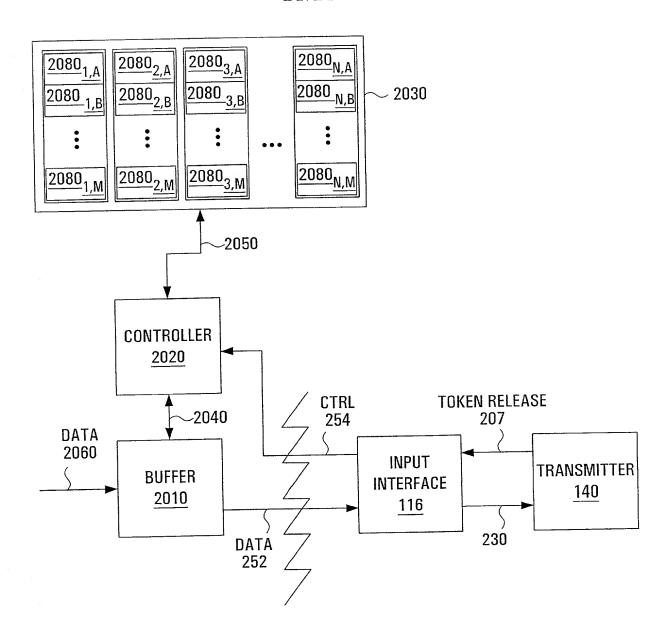


FIG. 20